

## **REMARKS**

Claims 1-24 were remain pending in the application. Claim 2 has been cancelled. Claims 1, 12, and 15 have been amended. Claim 25 has been added. Accordingly, Claims 1 and 3-25 are now pending in the application.

### **Specification:**

The examiner requested that the status of related U.S. applications and patents, and foreign application referenced in the specification be updated. Applicant notes that the status of the referenced applications and patents has not changed. Accordingly, no amendments to the specification have been made in this regard.

### **Section 102(b) Rejections:**

Claims 1-2 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bannon et al. (U.S. Patent Number 5,987,544).

Bannon, column 4, lines 43-47, describes a duplicate tag store 28, which “contains bits corresponding to valid, shared and dirty for each tag address entry. By providing a provision for storing dirty bits in the duplicate tag store, less interrupts are necessary to determine the complete status of a block of data in the BCACHE 24”. At column 4, lines 62-65, a “processor 13a reads the other processors 13b, 13c duplicate tag stores 28b, 28c to determine if the block desired by the requesting processor 13a is resident in the processors 13b, 13c backup cache” 24 and its status. And at column 3, lines 49-56, “This improves system performance since the processor bus and processor are not occupied with unnecessary tasks such as informing other processor of the status of its higher level caches. Moreover, by providing a separate index bus to the backup cache the index bus can be used to continue to process requests from the processor for private reads and writes”.

Additionally, Applicant submits that Bannon teaches, in the Abstract,

“A computer system includes a plurality of processor modules coupled to a system bus with each of said processor modules including a processor interfaced to the system bus. The processor module has a backup cache memory and tag store. An index bus is coupled between the processor and the backup cache and backup cache tag store with said bus carrying only an index portion of a memory address to said backup cache and said tag store. A duplicate tag store is coupled to an interface with the duplicate tag memory including means for storing duplicate tag addresses and duplicate tag valid, shared and dirty bits. The duplicate tag store and the separate index bus provide higher performance from the processor by minimizing external interrupts to the processor to check on cache status and also allows other processors access to the processor's duplicate tag while the processor is processing other transactions.” (Emphasis added) (See also Column 3, lines 30-57)

Applicant respectfully submits that Bannon fails to teach or suggest, “a control logic operable to read the redundant copies of a dirty indicator from storage and to treat the block of memory associated therewith as dirtied if all or any one of the redundant copies of the dirty indicator has the predetermined state” as recited in claim 1. Applicant submits that tags in the BCACHE are used by the processor for instruction execution and tags in the duplicate tag store are provided to inform other processors of the status of tags in the BCACHE.

In accordance, claim 1 is believed to patentably distinguish over Bannon. Claim 2 depends on independent claim 1 and is therefore believed to patentably distinguish over Bannon for at least the reasons given above.

Furthermore, independent claim 12 recites features similar to those highlighted above with regard to independent claim 1 and are therefore believed to patentably distinguish over Bannon for at least the reasons given in the above paragraphs discussing claim 1.

Also, Applicant respectfully requests examination of added Claim 25, which is believed to patentably distinguish over the cited references.

**Section 103(a) Rejections:**

Claims 3-10 and 13-14 were rejected under U.S.C. § 103(a) as being unpatentable over Bannon in view of Garnett (U.S. Patent Number 5,991,900). Claims 3-10 and claims 13-14 are dependent upon claim 1 and claim 12, respectively, and are believed to patentably distinguish over the Bannon and Garnett, whether alone or combined, for at least the reasons given in the above paragraphs discussing claim 1 and claim 12.

In addition, Claims 15-23 were rejected under U.S.C. § 103(a) as being unpatentable over Garnett in view of Bannon.

Applicant respectfully submits that Garnett and Bannon, whether alone or combined, fail to teach or suggest, “each cycle including reading the redundant copies of a dirty indicator from storage and treating a block of memory associated with the redundant copies as dirtied if all or any one of the redundant copies of the dirty indicator has the predetermined state” as recited in claim 15. In accordance, claim 15 is believed to patentably distinguish over Garnett and Bannon, whether alone or combined. Claims 16-23 depend on independent claim 15 and are therefore believed to patentably distinguish over Garnett and Bannon, whether alone or combined, for at least the reasons given above.

Also, Claim 11 was rejected under U.S.C. § 103(a) as being unpatentable over Bannon in view of Watt (U.S. Patent Number 6,272,033). Claim 11 is dependent upon claim 1, and is believed to patentably distinguish over Bannon and Watt, whether alone or combined, for at least the reasons given in the above paragraphs discussing claim 1.

Furthermore, Claim 24 was rejected under U.S.C. § 103(a) as being unpatentable over Garnett in view of Bannon and in further view of Watt. Claim 24 is dependent upon claim 15, and is believed to patentably distinguish over Garnett, Bannon, and Watt, whether

alone or combined, for at least the reasons given in the above paragraph discussing claim 15.

### CONCLUSION

In light of the foregoing amendments and remarks, Applicants submit that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-03100/BNK.

Respectfully submitted,



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